

## REMARKS

This Amendment is filed in response to the Office Action dated Feb. 4, 2003. Claims 11 and 18 have been amended. Claims 4, 6-9, 12-17, 21-22 and 27 were withdrawn from consideration. Claims 1-27 are currently pending. Reexamination and reconsideration are respectfully requested.

Applicant notes that claim 4 depends from claim 1 and claims 12-14 depend from claim 11. If claims 1 and 11 are allowed, then applicant will request that these dependent claims be examined.

Claims 18-19 were rejected under 35 U.S.C. 112, second paragraph. Applicant does not agree with the Examiner that the original claim language is indefinite. However, to expedite prosecution, applicant has amended claim 18. Support for the amendment is found in the specification, for example, at page 18, lines 4-10. Applicant respectfully submits that claim 18 and claim 19 (which depends from claim 18) comply with section 112.

Claims 1, 3, 11, 18 and 20 were rejected under 35 U.S.C. 102(e) as unpatentable over U.S. Patent No. 6,274,907 to Nakagawa et al. (hereinafter "Nakagawa"). The rejection is respectfully traversed. Applicant respectfully submits that the Examiner has cited no portion of Nakagawa that describes or suggests a semiconductor device in which "a conduction layer is provided above the floating gate, and the conduction layer entirely overlaps the floating gate" as recited in claim 1. The Examiner cited Figs. 21a and 24a for a conduction layer 76a and a floating gate 31. Applicant is unsure what the Examiner is referring to by reference number 76a. The Figures cited by the Examiner do not appear to include a reference number 76a. The Examiner may have intended to cite reference number 81 instead of 76a. If so, then applicant further directs the Examiner's attention to Figs. 1 and 21b. As described in Nakagawa, Fig. 21a and 21b are cross-sectional views taken along the lines A-A' and B-B' in Fig. 1. Fig. 21b appears to show a location where layer 81 does not overlap any portion of the floating gate layer 31, because layer 81 does not appear in Fig. 21b. From Figs. 1, 21a, 21b, it is clear that layer 81 extends over only a portion of the floating gate instead of being positioned so that it "entirely overlaps the floating gate" as recited in claim 1. Accordingly, applicant respectfully requests that the rejection of claim 1 over Nakagawa be withdrawn.

Regarding claim 3, the Examiner again cited layers 76a and 31 in Figs. 21 and 24. Claim 3 depends from claim 1 and is patentable over the cited art for at least the same reasons as claim 1. In addition, applicant respectfully submits that the Examiner cited no portion of Nakagawa that describes or suggests "a side end of the conduction layer formed above the floating gate and an end of the floating gate are aligned with each other" as recited in claim 3. The relationship of layer 81 to layer 31 in Nakagawa does not appear to include a structure in which "a side end of the conduction layer" and "an end of the floating gate are aligned with each other" as recited in claim 3. Accordingly, for at least the above reasons, applicant respectfully requests that the rejection of claim 1 over Nakagawa be withdrawn.

Regarding claim 11, applicant respectfully submits that the Examiner has cited no portion of Nakagawa that recites a device "wherein at least a portion of the conduction layer is located vertically above the floating gate along the entire length of the floating gate, and a width of the conduction layer located vertically above the floating gate is formed to be greater than a width of the floating gate" as recited in claim 11. Applicant notes that the configuration of the layers of Nakagawa as cited by the Examiner do not appear to show a structure in which the conduction layer is both located "along the entire length of the floating gate" and includes "a width" that is "greater than a width of the floating gate" as recited in claim 11. Accordingly, applicant respectfully submits that the rejection of claim 11 over Nakagawa be withdrawn.

Claim 18 depends from claim 1 and is patentable over the cited art for at least the same reasons as claim 1.

Claim 20 depends from claim 10, which was not rejected over Nakagawa by the Examiner. Applicant respectfully submits that the Examiner cited no portion of Nakagawa that describes or suggests a structure "wherein a conduction layer is provided vertically above the floating gate at least in a region where the control gate is not disposed vertically above the floating gate" as recited in claim 10, from which claim 20 depends. The Examiner cited Fig. 24a, which appears to show no region where "the control gate is not disposed vertically above the floating gate." Accordingly, applicant respectfully requests that the rejection of claim 20 over Nakagawa be withdrawn.

Claims 1 and 5 were rejected under 35 U.S.C. 102(b) as unpatentable over U.S. Patent No. 6,100,579 to Sonoda et al. ("hereinafter "Sonoda"). The rejection is respectfully traversed.

Applicant respectfully submits that the Examiner cited no portion of Sonoda that describes or suggests a semiconductor device in which "a conduction layer is provided above the floating gate, and the conduction layer entirely overlaps the floating gate" as recited in claim 1. The Examiner cited Fig. 13 and reference number 58 for a conduction layer and reference number 52 as the floating gate. Applicant further directs the Examiner's attention to Sonoda Fig. 7. Fig. 7 appears to show locations where layer 58 does not overlap any portion of the floating gate layer 52. Thus, applicant submits that it is clear that layer 58 is not positioned so that it "entirely overlaps the floating gate" as recited in claim 1. For example, as seen in Fig. 7, the layer 58 appears to extend over only a portion of the layer 52 instead of being positioned to "entirely overlap" the layer 52. Accordingly, applicant respectfully requests that the rejection of claim 1 over Sonoda be withdrawn.

Claim 5 depends from claim 1 and is patentable over Sonoda for at least the same reasons as claim 1.

Claims 23 and 24 were rejected under 35 U.S.C. 102(b) as unpatentable over U.S. Patent No. 5,959,879 to Koo (hereinafter "Koo"). The Examiner also appears to have rejected claims 1, 10 and 25-26 under 35 U.S.C. 102(b) as unpatentable over Koo. The rejection is respectfully traversed.

Applicant respectfully submits that the Examiner cited no portion of Koo that describes or suggests a semiconductor device in which "a conduction layer is provided above the floating gate, and the conduction layer entirely overlaps the floating gate" as recited in claim 1. The Examiner cited Figs. 2 and 4 and reference number 118 for a conduction layer and reference number 112 as the floating gate. Applicant further directs the Examiner's attention to Koo Fig. 4. Fig. 2 is a cross-sectional view along the line 2-2' of Fig. 4. As seen in Fig. 4, the line 2-2' extends through the layer 118. However, Fig. 4 also appears to show locations where layer 118 does not overlap any portion of the control electrode layer 116 (the floating gate electrode layer 112 is located below layer 116, as seen in Fig. 4). Thus, applicant submits that it is clear that layer 118 is not positioned so that it "entirely overlaps the floating gate" as recited in claim 1. Similar to the other references described above, as seen in Fig. 4, the layer 118 appears to extend over only a portion of the floating gate instead of being positioned so that it "entirely overlaps"

the floating gate. Accordingly, applicant respectfully requests that the rejection of claim 1 over Koo be withdrawn.

Regarding claim 10, applicant respectfully submits that the Examiner cited no portion of Koo that describes or suggests a structure "wherein a conduction layer is provided vertically above the floating gate at least in a region where the control gate is not disposed vertically above the floating gate" as recited in claim 10. The Examiner cited Fig. 2, which appears to show no region where "the control gate is not disposed vertically above the floating gate." Accordingly, applicant respectfully requests that the rejection of claim 10 over Koo be withdrawn.

Regarding claim 23, applicant respectfully submits that the Examiner has cited no portion of Koo that describes or suggests a device including a structure "wherein a line normal to any portion of the upper surface will contact at least one of the one or more conduction layers over the floating gate" as recited in claim 23. As noted above, as illustrated in Fig. 4, for example, there are regions between the layers 118 where "a line normal to . . . the upper surface" will not "contact at least one of the one or more conduction layers over the floating gate." Accordingly, applicant respectfully requests that the rejection of claim 23 over Koo be withdrawn.

Regarding claim 24, applicant respectfully submits that the Examiner cited no portion of Koo that describes or suggests a device wherein "a portion of the conduction layer is positioned vertically above the floating gate, where the portion of the conduction layer overlaps the entire floating gate" as recited in claim 24. The Examiner cited Figs. 2 and 4 in a similar manner as above for claim 1. For similar reasons to those described above for claim 1, applicant submits that Koo does not show that "the portion of the conduction layer overlaps the entire floating gate." Accordingly, applicant respectfully requests that the rejection of claim 24 over Koo be withdrawn.

Regarding claim 25, applicant respectfully submits that the Examiner cited no portion of Koo that describes or suggests a method including "forming a conduction layer vertically above the floating gate at least in a region where the control gate is not disposed vertically above the floating gate" as recited in claim 25. The Examiner cited Fig. 2, which appears to show no region where "the control gate is not disposed vertically above the floating gate." Accordingly, applicant respectfully requests that the rejection of claim 25 over Nakagawa be withdrawn.

Claim 26 depends from claim 25 and is patentable over Koo for at least the same reasons as claim 25.

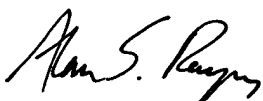
Claim 2 was rejected as unpatentable under 35 U.S.C 103(a) as unpatentable over Koo. The rejection is respectfully traversed. Claim 2 depends from claim 1 and is patentable for at least the same reasons as claim 1.

The Office Action also included various comments concerning the art and the non-patentability of features in various of the above mentioned claims. Applicants respectfully disagree with the Examiner's non-patentability conclusions. The discussion above has directly addressed some of those comments and the Examiner's other comments are deemed moot at this time in view of this response.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

In view of the above, examination of the present application on the merits is respectfully requested. Should the Examiner wish to discuss this application, the Examiner is requested to call the undersigned at the telephone number listed below.

Respectfully submitted,



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Alan S. Raynes  
May 5, 2003  
(Date)

**Version With Markings to Show Changes Made**

Claims 11 and 18 were amended as follows:

11. (amended)        A semiconductor device having a non-volatile memory transistor, comprising a non-volatile memory transistor including a semiconductor layer, a floating gate disposed above the semiconductor layer, and a control gate formed above the floating gate, wherein a conduction layer is provided above the non-volatile memory transistor and at least a portion of the conduction layer is located vertically above the floating gate along the entire length of the floating gate, and a width of the conduction layer located vertically above the floating gate is formed to be greater than a width of the floating gate.

18. (amended)        A semiconductor device having a non-volatile memory transistor according to claim 1, wherein the non-volatile memory transistor comprises a first circuit region, and wherein the semiconductor device further comprises a second circuit region, wherein the first circuit region and the second circuit region are formed in a sea of gates structure [mix-mounted therein].